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Influence of Asymmetric Contact Form on Contact Resistance and Schottky Barrier, and Corresponding Applications of Diode

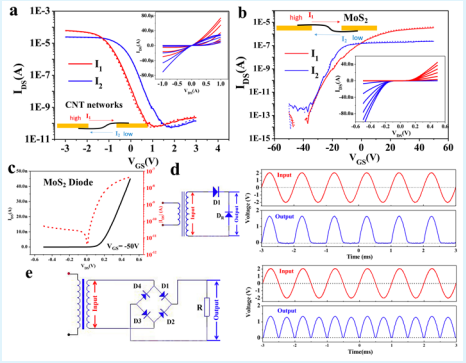
Yudan Zhao,[†,‡] Xiaoyang Xiao,[†,‡] Yujia Huo,[†,‡] Yingcheng Wang,[†,‡] Tianfu Zhang,[†,‡] Kaili Jiang,[†,‡] Jiaping Wang,[†,‡] Shoushan Fan,[†,‡] and Qunqing Li*[,†,‡]

[†]State Key Laboratory of Low-Dimensional Quantum Physics, Department of Physics and Tsinghua-Foxconn Nanotechnology Research Center, Tsinghua University, Beijing 100084, China

[‡]Collaborative Innovation Center of Quantum Matter, Beijing 100084, China

Supporting Information

ABSTRACT: We have fabricated carbon nanotube and MoS_2 field-effect transistors with asymmetric contact forms of source−drain electrodes, from which we found the current directionality of the devices and different contact resistances under the two current directions. By designing various structures, we can conclude that the asymmetric electrical performance was caused by the difference in the effective Schottky barrier height (Φ_{SB}) caused by the different contact forms. A detailed temperature-dependent study was used to extract and compare the Φ_{SB} for both contact forms of CNT and MoS_2 devices; we found that the Φ_{SB} for the metal-on-semiconductor form was much lower than that of the semiconductor-on-metal form and is suitable for all p-type, n-type, or ambipolar semiconductors. This conclusion is meaningful with respect to the design and application of nanomaterial electronic devices. Additionally, using the difference in barrier height caused by the contact forms, we have also proposed and fabricated Schottky barrier diodes with a current ratio up to 10^4; rectifying circuits consisting of these diodes were able to work in a wide frequency range. This design avoided the use of complex chemical doping or heterojunction methods to achieve fundamental diodes that are relatively simple and use only a single material; these may be suitable for future application in nanoelectronic radio frequency or integrated circuits.



KEYWORDS: *carbon nanotube, MoS_2, contact form, Schottky barrier, diode*

INTRODUCTION

Because of their unique electrical, optical, mechanical, and chemical properties, low-dimensional semiconducting materials have attracted tremendous interest and have been studied widely all over the world in the past few years. Among them, the one-dimensional semiconducting carbon nanotube (CNT) and two-dimensional few-layer molybdenum sulfide (MoS_2) are two of the most attractive semiconducting materials and have been considered as candidates for the conductive channel of future field-effect transistors (FETs) (or thin film transistors (TFTs)) in nanoelectronic applications[1−6] because of their great current capacity,[7] high mobility,[8,9] large on/off current ratio,[10,11] and even outstanding mechanical performance.[12,13] However, there are still some obstacles that need to be solved before their real use and manufacture, one of which is the performance limitation of metal−semiconductor contacts,[9,14,15] including contact materials[16−18] and contact forms.[19−21] To now, the focus has concentrated on evaluating and studying metal−semiconductor contacts by comparing various electrode materials for both CNT and MoS_2 devices, but not much attention has been paid to comparing the metal−semiconducting contact forms carefully, including semiconductor-on-metal (S-on-M) and metal-on-semiconductor (M-on-S) or embedded forms, an area which is also decisive and worthy of discussion.[22,23] Moreover, the relevant contrasting experiments with respect to contact forms are limited and the point of view is not uniform;[14,16] thus, a thorough experimental study on the contact forms is necessary.

Different from conventional bulk silicon technology, it is difficult to realize controllable and stable doping in nanomaterials. Thus, the diode, an important basic electronic component in the modern semiconducting industry, cannot be achieved by controlled doping of a p−n junction in nanodevices, which is currently the most widely used technology for diodes. Recently, there have been some nanomaterial diodes fabricated using a heterojunction method,[24−27] asymmetric electrode materials method,[28−34] and chemical doping method,[35−37] but a simpler fabrication technology and even the use of a single material remain barriers to achieving diodes for future large-scale nanoelectronic manufacture.

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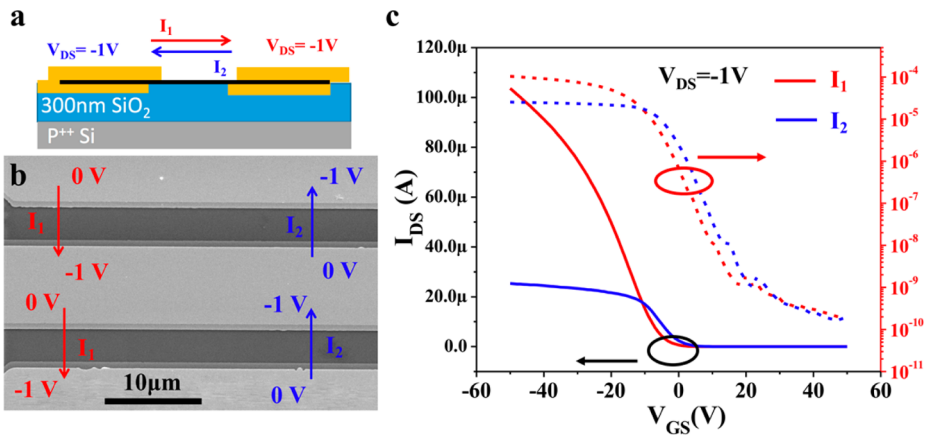

Figure 1. (a) Schematic and (b) scanning electron microscope images of the embedded double-layer electrode CNT-TFT. An obvious deviation in the two layers can be seen. (c) Transfer curves under V_{DS}= −1 V for the same TFT under different current directions show a large difference.

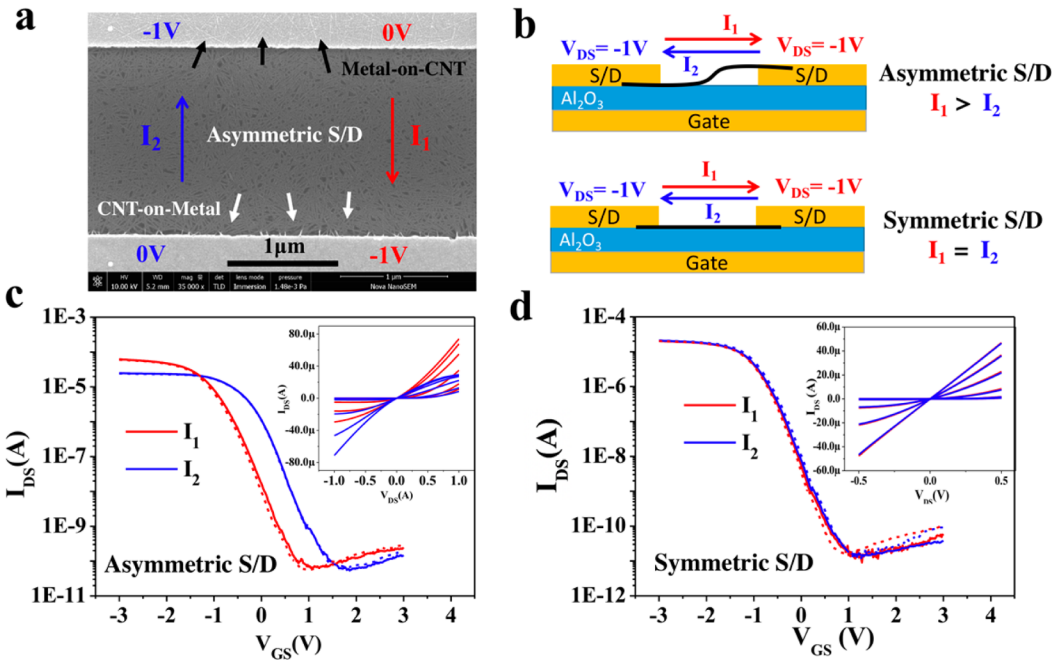

Figure 2. (a) SEM image and (b) schematics and (c) transfer and output characteristics of a typical local back-gate CNT-TFT with asymmetric contact forms. The drain current differs because of the direction. (d) Transfer and output characteristics of a typical local back-gate CNT-TFT with symmetric contact forms. No obvious directionality of the current is observed. Dashed lines here represent retest curves after exchanging the position of two cables and probes. All V_{DS}= −1 V here.

Therefore, to further study these two aspects, we fabricated one kind of asymmetric transistor based on either CNT and MoS_2, in which the source and drain (S-D) electrode material is the same but their contact forms are different, e.g., the source is S-on-M and drain is M-on-S, in the same transistor. We found that the asymmetric contact forms could lead to an asymmetric electrical performance if we exchanged the position of S and D (the bias voltage position), which means the device has directionality. Thus, to determine the influence of the contact forms on the electronic performance, the transfer length method (TLM)[14,16,38] and *Y*-function method (YFM)[39−41] were used to compare and calculate the contact resistance (R_c) of the same device under different current directions; also, a detailed temperature-dependent study that considered both thermionic emission over the Schottky barrier and thermally assisted tunneling was used to extract the effective Schottky barrier height (Φ_{SB})[17,42−44] of the two different contact forms using the same device. As a result, we found that the contact resistance showed a difference of approximately four times (5 and 20 kΩ) when the current flowed from the M-on-S to S-on-M electrode or vice versa, which denotes a different current direction for the asymmetric CNT-TFT; the effective Schottky barrier heights of CNT-on-metal and metal-on-CNT, as well as MoS_2-on-metal and metal-on-MoS_2, were 114 and 86 meV, and 95.4 and 32.4 meV, respectively. These results indicate that the contact form can influence the electrical performance to a large extent, and the Schottky barrier was concluded to be the determining mechanism, caused by different contact forms, by comparison of several device structures, no matter how long the contact length is or whether it is embedded or not. The conclusion that the Φ_{SB} of the metal-on-semiconductor form is much lower than that of the semiconductor-on-metal form means that it is widely suitable for all p-type, n-type, or

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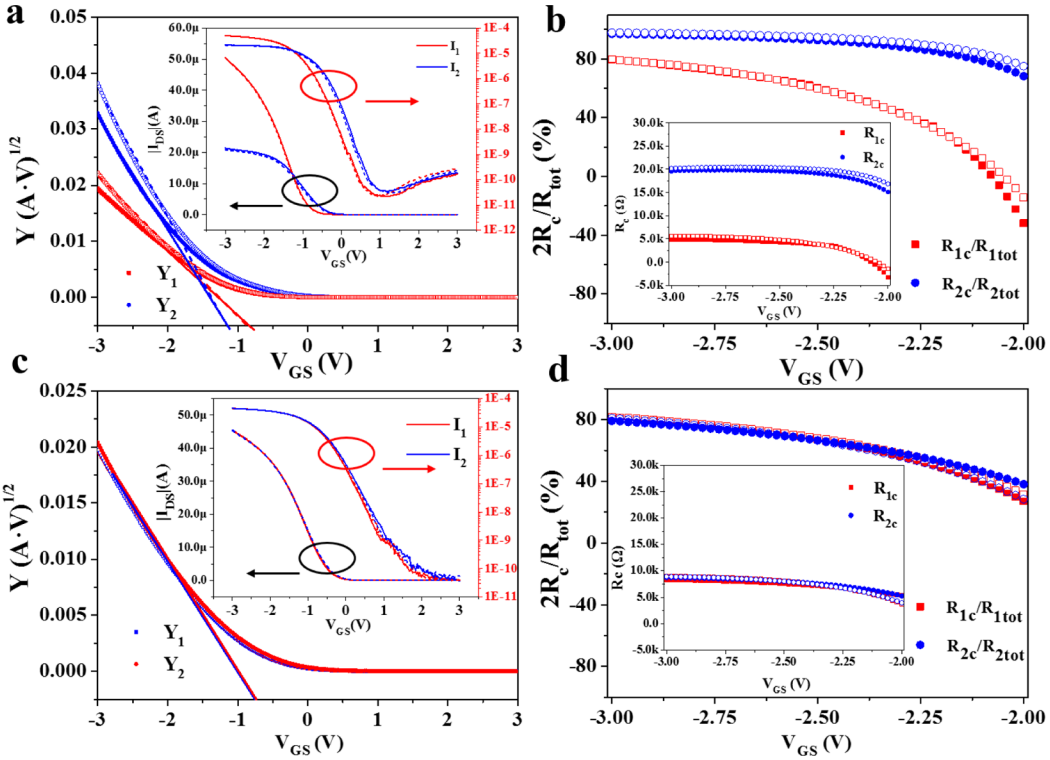

Figure 3. Contact resistance calculated by the *Y*-function method. (a) Transfer characteristics and corresponding *Y*-function of a typical CNT-TFT with asymmetric contact. (b) Contact resistance and the percentage of $2R_c/R_{tot}$ of the asymmetric device under two different directions. A difference in R_c of approximately four times and a 20% difference in $2R_c/R_{tot}$ reveal the tremendous influence of the contact forms. (c) Transfer characteristics and *Y*-function and (d) R_c and $2R_c/R_{tot}$ of a typical symmetric contact CNT-TFT. There is absolutely no difference in electrical performance between the two directions. Dashed lines here also represent retest curves after exchanging the cables and probes. All V_{DS}= −1 V for transfer curves here.

ambipolar semiconductors, which is helpful with respect to device design and fabrication.

Meanwhile, taking notice of the different Schottky barrier heights under different contact forms, we also proposed and fabricated a Schottky barrier diode using the asymmetric contact form and applied it in half-wave and full-wave rectifying circuits. The current ratio of the diodes was up to approximately 10^4 under V_{DS} ranges from −3 to 3 V, and rectifying circuits could work normally under a wide input frequency range. This easy processing method can solve diode application problems in future nanoelectronic radio frequency or integrated circuits, avoiding the use of complex chemical doping or heterojunction methods.

RESULTS AND DISCUSSION

We used a deposited semiconducting CNT network[45] and few-layer MoS_2 as conductive channel materials to study the influence of contact forms. Because the experimental phenomena associated with MoS_2 fabricated by both chemical vapor deposition (CVD) growth and mechanical exfoliation are the same, here we only demonstrate the results of mechanically exfoliated MoS_2.

We first found the asymmetric phenomena of CNT-TFTs through the double-layer source and drain electrode structure with global back-gate as shown in Figure 1; the thickness of the thermal SiO_2 dielectric layer is 300 nm. Although the embedded contact form is almost the same for both S and D, which occupies most of the contact region, there is a large current difference in the same TFT under different current directions, as the red and blue transfer curves in Figure 1c show. We suggest that the unavoidable deviation of the two layers of electrodes caused by the error in standard photolithography, which leads to opposing contact forms at the edge of the S and D electrodes, causes the asymmetric electrical properties, as the schematic and scanning electron microscope images in Figure 1a,b show.

To verify the influence of the different contact form on the electrical performance of TFTs, we fabricated simpler and more particularly asymmetric TFTs with both CNT networks and MoS_2, as shown in Figure 2 and Supporting Information Figure S1. Figures 2a and S1a show images of the asymmetric devices using a CNT network and MoS_2 as channels, respectively, in which the bottom contact is S-on-M and the top is M-on-S. Normally, for a conventional symmetric contact form, as Figures 2d and S1c show, the transfer characteristics should be absolutely the same, no matter which side is selected as S (or D). However, for the asymmetric transistors shown in Figures 2c and S1b, the transfer curves show obvious differences when the source position is exchanged from one side to the other side (which means the current direction is exchanged). Schematics of CNT-TFTs and corresponding current direction in Figure 2b describe this phenomenon clearly. In this work, we used V_{DS} = −1 V for p-type CNT devices and V_{DS} = 1 V for n-type MoS_2 devices. To distinguish the two different current directions, we have labeled the larger current (I_1) of both CNT and MoS_2 devices with red curves and arrows and have used blue curves and arrows to indicate the smaller one (I_2); similar notation is used throughout. While the corresponding calculations under the I_1 direction are all red curves and that of the I_2 direction are all blue curves, for both CNT and MoS_2 throughout.

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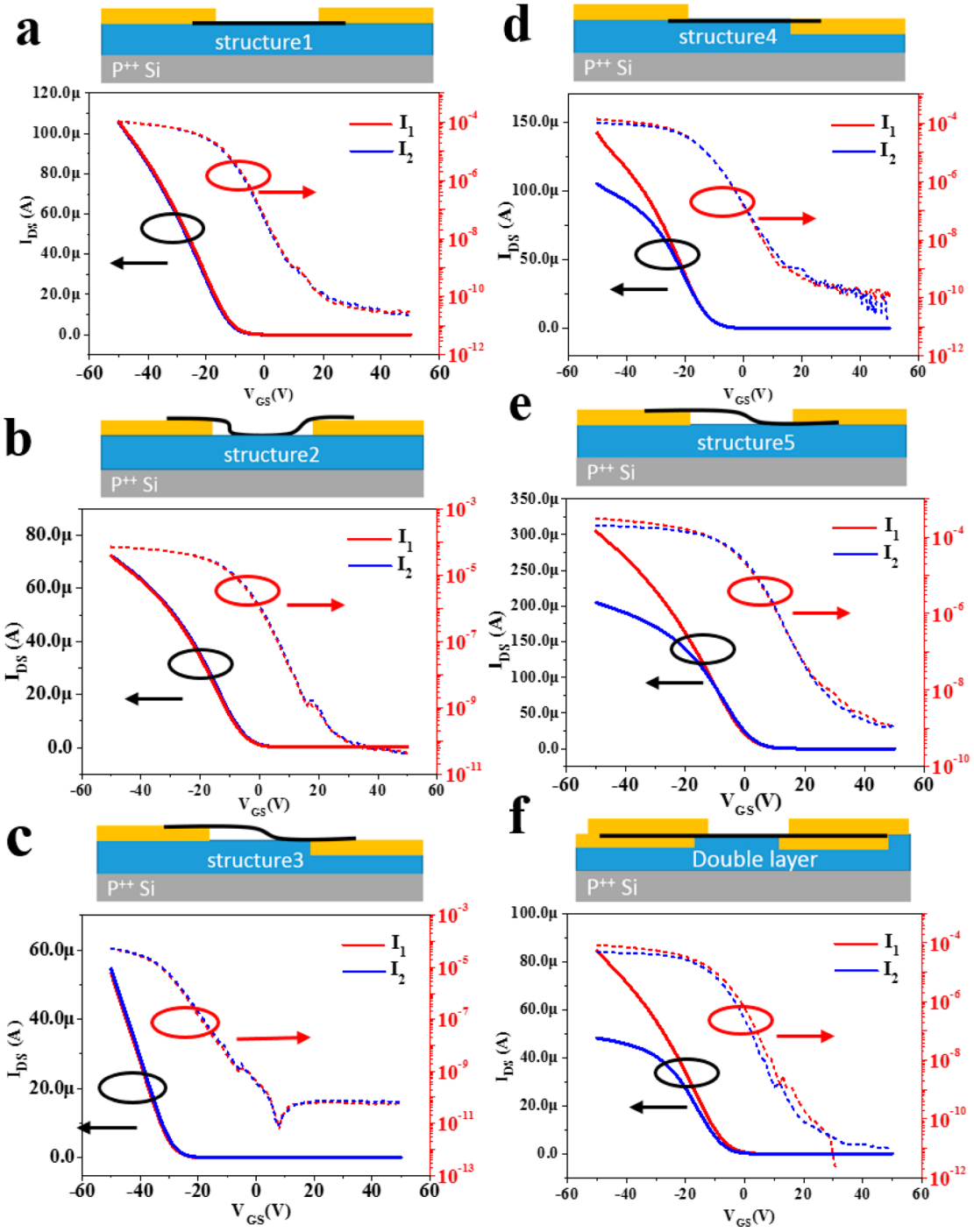

Figure 4. Comparison of transfer characteristics for six different structures (V_{DS}= −1 V here). Symmetric contact forms with (a) both M-on-S and (b) both S-on-M do not show current directionality. (c) When both contact forms are S-on-M but one side of the channel is suspended, there is no electrical difference. (d) When the contact forms are different but have no unilateral suspended channel, asymmetric electrical performance is exhibited, which indicates that contact form is the dominant cause, not the unilateral suspended channel. (e) Typical asymmetric contact forms show distinctions in the on current. (f) A double-layer S-D electrode with a tiny deviation shows electrical asymmetry, proving the mechanism caused by contact forms is due to the Schottky barrier of the semiconductor−metal contact edge, not the difference in the overlapping main contacting area. The SiO_2 dielectric in c, d, and f was etched by CF_4 to bury the electrodes, the depth of which is 50 nm.

Comparing the CNT and MoS_2 FETs, it is apparent that the larger current direction for p-type CNT FETs flows from the electrode of M-on-S to S-on-M, while that of the MoS_2 devices is the opposite; this will be explained by the difference between electrons and holes later.

Before analyzing the mechanism of the asymmetric electrical performance, the probable influence of probes and cables needs to be prevented. We therefore exchanged the two probe positions and tested the device again, achieving the same results, as the dashed lines in Figure 2 show (similar notation is also used throughout), which indicates that the asymmetric electrical performance is primarily caused by the structure, not instrument error.

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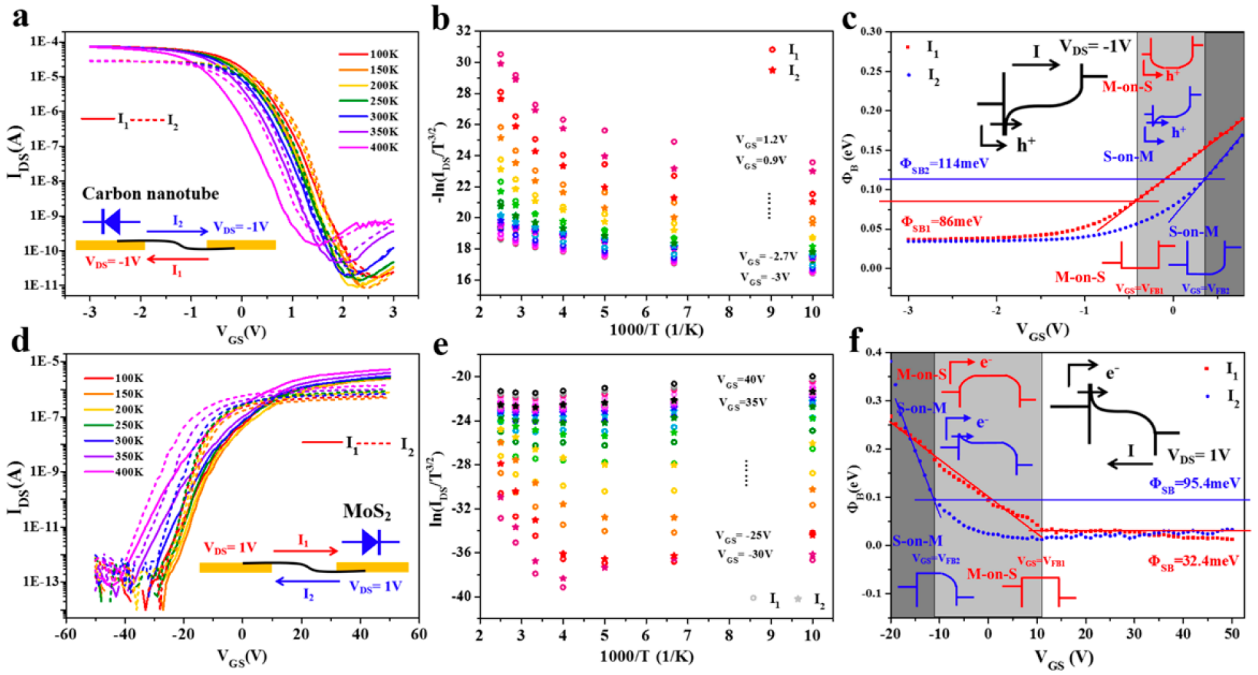

Figure 5. Transfer characteristics of a typical (a) CNT-TFT and (d) exfoliated MoS_2 FET with different current directions (labeled by solid lines and dashed lines) under various temperatures from 100 to 400 K. $\ln(I_d/T^{3/2})$ versus $1000/T$ under different gate biases extracted from transfer curves of (b) CNT-TFT and (e) MoS_2−FET in both directions. The slope of dots with the same gate bias (in the same color) in the high-temperature area can be used to calculate the barrier height (Φ_B) under specific gate voltages. Φ_B for different gate biases of (c) CNT-TFT and (f) MoS_2−FET in the two current directions show different effective Schottky barrier heights and corresponding flat-band voltages. V_{DS}= −1 V for CNT-TFTs and V_{DS}= 1 V for MoS_2−FETs here.

With the CNT-TFT as an example, we extracted the contact resistance of the same device under different directions using the *Y*-function method. Each direction of the transistors was also tested twice before and after exchanging the position of probes and cables, as the filled dotted lines and hollow dotted lines in Figure 3 show. From the experimental data I_{DS}−V_{GS} curve, we can achieve the g_m−V_{GS} curve where $g_m = dI_{DS}/dV_{GS}$. Then we define the *Y*-function which can also be achieved through the tested I_{DS}−V_{GS} curve as[39]

$$Y = \frac{I_{DS}}{\sqrt{g_m}} = \sqrt{V_{DS}G_m}(V_{GS} - V_T) \quad (1)$$

where $G_m = (\mu_{FE}C_G)/L_{ch}^2$ is defined as the transconductance parameter, which can be calculated by the slope k of the linear region of the *Y*-function, as $G_m = k^2/V_{DS}$, and threshold voltage V_T can be extracted from the V_{GS}-axis intercept of the linear region of the *Y*-function. Finally, using the formula[39]

$$\begin{aligned} 2R_{C,S} &= R_{total} - R_{ch} \\ &= \frac{V_{DS}}{I_{DS}} - \frac{L_{ch}^2}{\mu_{FE}C_G(V_{GS} - V_T)} \\ &= \frac{V_{DS}}{I_{DS}} - \frac{1}{G_m(V_{GS} - V_T)} \end{aligned} \quad (2)$$

we can calculate R_c using the *Y*-function, which can be achieved only using the transfer characteristic curves, and avoid measuring specific parameters of the transistors. From the *Y*-function in Figure 3a, we find that the slopes of the linear region of the *Y*-functions are different, leading to a difference in R_c of approximately four times for these two directions. Similarly, we also define the contact resistance of the I_1 direction as R_{c1} and that of I_2 as R_{c2}. Figure 3b shows that R_{c1} is approximately 5 kΩ, while R_{c2} is approximately 20 kΩ under the on state; and R_{c1} possesses less than 80%, while R_{c2} possesses greater than 95%, of the total device resistance (R_{tot}) under the on state. On the other hand, no distinction can be found in symmetric devices, as the *Y*-function and R_c in Figure 3c,d show.

The results indicate an enormous influence on R_c by the contact forms. Although the current flows through both source and drain electrodes no matter the direction, the R_c we calculated still confirms that the current direction is decisive, so the asymmetric contact form affects the electrical performance greatly. However, the *Y*-function method can only determine the total contact resistance; it cannot distinguish which side plays a leading role. Additionally, it is doubtful that if the current difference is judged by the contact resistance, the current would be different under every gate voltage. However, the phenomena mainly reveal near the on-state, not in the off-state. Moreover, it is also important to understand the mechanism by which the contact form can influence the electrical performance of FETs. Thus, according to the basic experimental results above, a unilateral suspended semiconducting channel that cannot be modulated;,[46,47] a main-area contact difference caused by S-on-M or M-on-S in the metal and semiconductor contact region,[16,38,48] and a Schottky barrier difference near the metal-semiconducting contact edge[9,49−51] are the three possible mechanisms that may cause the directionality of devices.

Therefore, we designed CNT-TFTs with six structures to determine the mechanism behind the asymmetric electrical performance, as Figure 4 and Figure S5 in Supporting Information show. In each structure, we demonstrate a schematic of the structure, transfer curves of both current

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directions, and the change in resistance/current with various channel lengths under the on state (the TLM in Figure S5). Because the contact resistance of CNT network TFTs cannot be extracted by TLM accurately,[16] we only use it to compare the R_c qualitatively.

From Figure 4a,b, it is clear that the transfer curves of the two directions coincide perfectly under symmetric structures; there is also no distinction between the intercepts of the resistance−channel length lines, which suggests that there is no difference in $2R_c$, as Figure S5a,b shows. The structure in Figure 4c has only a unilateral suspended CNT channel with both S-on-M contact forms (the other one is a buried electrode), but it does not show asymmetric electrical performance, as do structures 1 and 2. In contrast, structure 4 in Figure 4d has no suspended channel but does have an S-on-M and an M-on-S contact, showing asymmetric transfer curves and R_c as we demonstrate above, as does the original structure 5 in Figure 4e. Therefore, we can conclude that the main mechanism that influences the electrical performance and leads to asymmetric FETs is not the suspension of the channels. Some studies have shown that the overlapping conducting region of metals and semiconductors could influence the performance of TFTs to a large extent because of the conductive length[15,38] or van der Waals gap.[22,23] Thus, we analyzed the CNT-TFT of structure 6 with a double-layer S-D as an embedded contact form, as Figure 4f shows, which is the same as that in Figure 1. In this structure, the main contact form of both S and D is almost the same and symmetric (M-on-S-on-M), as well as the contact resistance, contact length, or gap in the main contact region. However, because of unavoidable error in the photolithography process, the two-layer electrodes may have a tiny deviation, of approximately dozens or hundreds of nanometers, leading to a totally opposite contact form at the metal−semiconductor contact edge. Thus, the existence of asymmetric electrical performance in structure 6 reveals that the metal−semiconducting contact form near the asymmetric edge is the main mechanism, which means that the different contact Schottky barrier height here plays a leading role, not the main-area contact forms, even though their area is far larger than that of the asymmetric edges. Detailed images and analysis can be found in section 1 of the Supporting Information. It is also needs to be said that the phenomenon of asymmetric current mainly reveal near the on-state, not in the off-state. Thus, we believe the Schottky barrier is the real mechanism because the Schottky barrier becomes dominated only near on-state (when V_{GS} over the flat band, tunneling current plays the leading role), while the Schottky barrier is not dominated near the off-state (when V_{GS} below the flat band, thermionic current plays the leading role).

Next, since the Schottky barrier difference is suggested to be the main mechanism because of the contact forms, an accurate experiment based on the thermal emission and tunneling current theory dependence on temperature[52] for Schottky barrier devices is carried out to extract the effective Schottky barrier height for different contact forms.

Panels a and d of Figure 5 show the transfer characteristics of a typical CNT-TFT and exfoliated MoS_2 FET with different current directions under temperatures ranging from 100 to 400 K. According to the thermionic theory, when the gate voltage (V_{GS}) is below the flat-band voltage (V_{FB}), the drain current can be written as

$$I_d = A_{2d}^{*} T^{3/2} \exp\left(\frac{q\phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right] \quad (3)$$

where A_{2d}^{*} is the 2D equivalent Richardson constant (we consider the CNT network to be two-dimensional as well), T is the absolute temperature, k_B is the Boltzmann constant, q is the electron charge, and V_{ds} is the drain to source bias, i.e., 1 V for n-type MoS_2 and −1 V for p-type CNT transistors.[17,43,53] Therefore, the value of ln $(I_d/T^{3/2})$ under different temperatures can be drawn from the transfer curves under each gate bias voltage. Panels b and e of Figure 5 show the Arrhenius plot of $\ln(I_d/T^{3/2})$ versus $1000/T$ under different gate biases for CNT and MoS_2 transistors, respectively, and the barrier height under specific gate biases can be calculated by the slope of each line (dots in the same color) in the high-temperature region, in which the round dots represent $\ln(I_d/T^{3/2})$ with the current direction I_1, and stars represent that of I_2. Using the slopes of the high-temperature region we extracted, graphs of Φ_B versus gate bias voltage are drawn in Figure 5c,f for both CNT and MoS_2 transistors in both directions. For typical Schottky barrier devices, when V_{GS} is below V_{FB}, thermionic emission current plays the dominant role, while when V_{GS} becomes larger than V_{FB}, thermally assisted tunneling current becomes increasingly significant, resulting in nonlinear behavior. Therefore, Φ_{SB} can be most accurately extracted from the end of the linear region, where $V_{GS} = V_{FB}$.[17,43] After that, the on current is mainly decided by the tunneling current which is determined by the Φ_{SB} because of the pining of Schottky barrier, and the Φ_B of thermionic current should not be taken into consideration.

In Figure 5c, the red dotted lines are extracted from the transfer curve for the I_1 direction, which means that drain bias voltage (V_D = −1 V) is added to the CNT-on-metal electrode, while the blue dotted lines are extracted from that for the I_2 direction, where bias voltage is added to the metal-on-CNT electrode. Because the Schottky barrier primarily acts on the other source electrode side (V_S = 0 V), as the inner schematic of Figure 5c shows, we can obtain Φ_{SB} = 86 meV for the metal-on-CNT contact and Φ_{SB} = 114 meV for the CNT-on-metal contact. The height of Φ_{SB} exactly corresponds to the direction of the on current and R_c. Because the sweep direction of the local back-gated V_{GS} for the CNT-TFT here was from −3 to 3 V, the tunneling current dominates at first for both types, located in the white area of Figure 5c. As the gate bias moves in the positive direction, the energy band bends downward to the same extent for both directions,[54] but because of the lower Φ_{SB} for the metal-on-CNT side, V_{GS} could arrive at V_{FB} first, obstructing the tunneling current in the light-gray area in Figure 5c. For the blue type, because of the higher Φ_{SB} for the CNT-on-metal side, the V_{GS} here cannot bend the energy band to the flat band, thus tunneling current is still allowed in this area. As the V_{GS} moves in the positive direction enough for the V_{FB} of the CNT-on-metal side, thermal emission begins to play the principal role for both of them, as shown in the dark-gray area in Figure 5c. In summary, gate voltage here plays an important role of modulating the energy band as well as effective Schottky barrier to decide which kind of current takes the lead, and thus we can find the difference of drain current under the two directions is relevant to the gate voltage closely as a result.

Similarly, Figure 5f shows Φ_{SB} = 32.4 meV for the metal-on-MoS_2 contact and Φ_{SB} = 95.4 meV for the MoS_2-on-metal contact. The height of Φ_{SB} here also exactly corresponds to the

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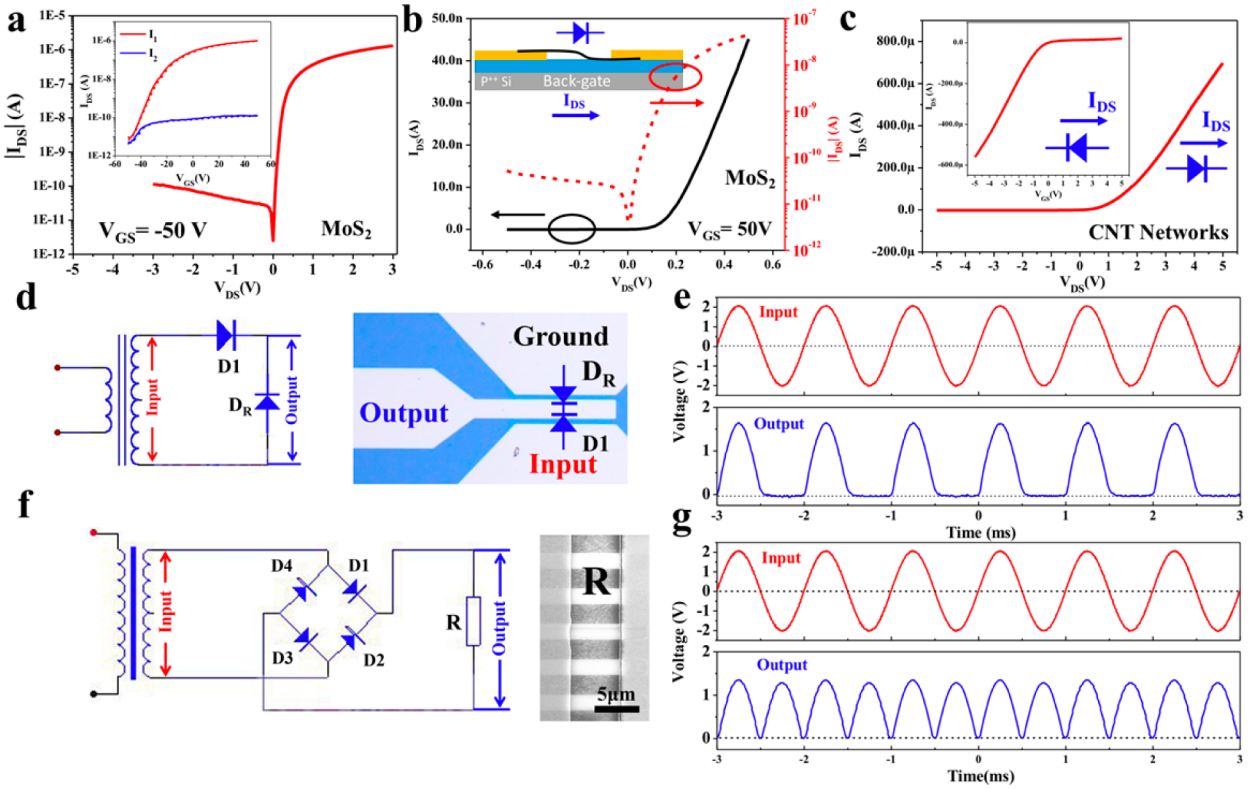

Figure 6. Schottky barrier diode achieved by asymmetric contact forms. (a) Transfer curves under two directions (V_{DS}= −1 V) and corresponding I−V curve of MoS_2 diode. The current ratio could be up to 10^4 when the sweep range is from −3 to 3 V under V_{GS} = 50 V. (b) MoS_2 diode can work normally when the bias voltage range decreases to −0.5 to 0.5 V under V_{GS} = 50 V and can keep a current ratio near 10^3. Inner schematic: Structure and direction of the MoS_2 diode, the global back-gate bias, can both be added or not. (c) CNT network diode with opposite bias voltage, showing inverse I−V curves, which means the diode is very reliable. The schematic and input−output waveforms of (d, e) half-wave rectifying circuits and (f, g) full-wave rectifying circuits consist of asymmetric contact diodes. Output voltages are both attenuated to some extent but not distorted. The small deviation between the two periods in full-wave rectifying circuits may be due to the slight inconformity of the diodes. Load resistance is fabricated and adjusted by cutting CNT thin films into strips.

direction of the on current and R_c. The global back-gate sweep direction of V_{GS} is from −50 to 50 V, which means the energy band bends upward at first and only thermal emission current can flow through, as seen in the dark-gray area in Figure 5f. As V_{GS} moves in the positive direction, the energy band bends downward and first meets the higher flat-band of the MoS_2-on-metal contact (blue type). Since then tunneling current begins to flow in the blue type while it is still blocked in the red type, as shown in the light-gray area of Figure 5f. Finally, after V_{GS} moves to the V_{FB} of the red type, both of the two types are primarily dominated by the tunneling current, arriving in the white area in Figure 5f.

The mechanism by which the metal−semiconductor junction configuration influences the effective SBH has been studied previously. In some recent reports, calculations of the interface interaction between the metal electrode and semiconductor have proved that junction geometry[55,56] can influence the SBH to a certain extent; and the substrate inhomogeneity which semiconductor located on (SiO_2 for M-on-S side and metal for S-on-M side here) can also affect the SBH.[57−59] Therefore, it is likely that the different metal−semiconductor junction configurations of the asymmetric contact transistor here lead to the different SBH. Further on, we believe the difference of van der Waals gap[22] between semiconductor and metal caused by their relative location could lead to different effective Schottky barrier heights, which is caused by the interaction between metal−semiconductor and substrate inhomogeneity mentioned above. Normally, the Schottky barrier height is only judged by the work functions of metal and semiconductor, but here the different interaction between them caused by different junction geometry can lead to different effective SBH.

The experiments and analysis illustrated above confirm that the effective Schottky barrier height of the S-on-M contact form is higher than that of the M-on-S for both n-type and p-type devices. Moreover, as we proposed above in Figure 2 and Figure S1, the phenomenon in which I_1 and I_2 of the CNT-TFT and MoS_2−FET show opposing properties can be explained now because electrons in n-type devices and holes in p-type devices have similar transmission properties, while the same direction of electron transport and hole transport could lead to a converse current direction. This is why the larger current of CNT-TFT flows from M-on-S to S-on-M, while that of MoS_2−FET flows in the opposite direction.

Furthermore, asymmetric contact form FETs with CNT aligned arrays and single CNTs as conductive channels with global back-gates were also fabricated to verify the experiments and theory we proposed above, as Figure S4 in section 3 of the Supporting Information demonstrates. Because the FETs show ambipolar properties, both electrons and holes could be transported in channels under the two branches. The result is that both of the branches confirm the current phenomena of p-type and n-type devices, which indicates that the theory of the Schottky barrier difference caused by the contact forms is correct and widely suitable, even for ambipolar devices.

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Table 1. Performance and Fabrication Processes Comparison of Diodes Based on Low-Dimensional Semiconductors[24,25,28−32,36,60,64,65]

Type of diodes	Maximum Current ratio	I_{on}(A)	Large-scale	No chemical doping	No electron-beam lithography	No Site-directed transfer
Asymmetric contact forms (CNT and MoS_2)	**>10^4**	**~2x10^{-6}**	✔	✔	✔	✔(CNT)
MoS_2 heterojunction diodes [24, 25, 65]	10~10^3	~10^{-6}	✘	✔	✘	✘
Asymmetric S/D metals (CNT)[28-31, 34]	10^2~10^4	~1x10^{-6}	✘	✔	✘	✔
Split-gate (CNT)[32]	**~10^7**	2x10^{-8}	✘	✔	✘	✔
Pt-Ti asymmetric S/D (MoS_2)[33]	<10^2	**2x10^{-6}**	✘	✔	✘	✔
Asymmetric thiolate molecules doping (CNT)[35]	**~10^4**	**~5x10^{-6}**	✘	✘	✘	✔
Intramolecular p-i-n junction diodes (CNT)[36]	10^2~10^3	~10^{-8}	✘	✘	✘	✔
Self-gating (CNT)[60]	**~10^6**	**5x10^{-6}**	✘	✔	✘	✔
Si_3N_4 asymmetric passivation (CNT)[64]	>10^2	**2x10^{-6}**	✘	✔	✘	✔

On the other hand, taking advantage of the difference in Schottky barrier because of the asymmetric contact transistors, we can fabricate a Schottky barrier diode using this property, as the schematic in Figure 6b shows; and the global back-gate bias can also be added or not. To amplify the effect of the barriers, we minimize the channel length down to 1−2 μm and add a global back-gate voltage to turn all CNTs and MoS_2 to the on state, achieving a high-performance Schottky diode, as shown in Figure 6a. Diodes without back-gate bias can also work well, which is shown in section 5 of the Supporting Information. Key electrical performance and fabrication processes of several recently reported low-dimensional semiconductor diodes are compared in Table 1, from which we can see that this method for high-performance diode fabrication is simpler and only involves a single conductive material, avoiding complex chemical doping or heterojunction methods.

Panels a and c of Figure 6 show the Schottky diode achieved by asymmetric contact forms with back-gate bias, using MoS_2 and CNT as conductive channels, respectively. The on current difference in the two directions could be up to approximately 10^4, so the current ratio is 10^4 under V_{DS} from −3 to 3 V, as Figure 6a shows. In Table 1, we can also find that the maximum current ratio and on current of our work are located in the top level among the recently reported diodes based on low-dimensional semiconductors, while the fabrication processes are able to be large scale and have no need of chemical doping, electron-beam lithography, or site-directed transfer, only with one kind of semiconductor and metal. The current ratio would decrease if the range of V_{DS} was reduced to 0.5 V, but it can still remain over 10^3, as Figure 6b shows. The asymmetric diodes can still work with current ratio between 10^2 and 10^3 without back-gate voltage as Figure S6 shows, which gives designers various choices to meet the specific needs. From Figure 6c, inverse $I-V$ curves of the CNT-based diode could be measured if we change the current direction, which means the direction of the diode is fixed. Additionally, we apply the diodes we designed into half-wave and full-wave rectifying circuits,[60] as Figure 6d−g show. Load resistance here is fabricated and adjusted by cutting CNT thin films into strips to meet our requirements. As a result, although the output waveforms are not distorted, they still have some attenuations (2 V down to 1.65 V for half-wave and 2 V down to 1.35 V for full-wave); the full-wave output also has a small deviation between the two periods of 0 to π and π to 2π. This could be caused by the circuit design and slight inconformity of our diodes. However, the diodes can still work normally under a wide range of frequency, from 0.1 to 50 kHz, which is an important foundation for primary element applications in future carbon nanotube (or 2D material) based nanoelectronic[61−63,66] integrated or radio frequency circuits.

CONCLUSIONS

In summary, we have systematically studied the influence of contact forms on electrical performance through asymmetric field-effect transistors based on CNTs and MoS_2, including transfer characteristics, the on current, contact resistance, and the Schottky barrier. By comparing various structures, we found the real mechanism of the contact forms was the difference in effective Schottky barrier height caused by the metal and semiconductor contact edge. Arrhenius plots were drawn through temperature-dependent studies to extract the Φ_{SB}, and it was found that for all p-type, n-type, or ambipolar semiconductors, the Φ_{SB} of the metal-on-semiconductor form was much lower than that of the semiconductor-on-metal form, leading to the directionality of asymmetric devices and opposing properties between transport phenomena of electrons and holes. Finally, taking advantage of the different barrier heights, we proposed and fabricated a Schottky barrier diode using the asymmetric structure, the current ratio of which could be as high as 10^4. Rectifying circuits consisting of the diodes could work normally under a wide frequency range, indicating the diodes are reliable for future applications of nanoelectronic integrated circuits. This method is simple and only requires a single material, avoiding the complex chemical doping and heterojunction methods, to achieve high-performance diodes.

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METHODS

Deposition of CNT Thin Films. Semiconducting SWCNT suspensions in methylbenzene (more than 99.9% pure) were prepared by preseparation of arc-discharged SWCNTs. Before deposition, the substrates were treated via O_2 plasma etching to functionalize the oxide surfaces and make them hydrophilic. Then, the samples were immersed in the semiconducting nanotube suspension for several hours to deposit the SWCNT random network thin films on the substrate. Finally, the substrate was refloated and dried using N_2. CNT aligned arrays and single-CNT channels were grown by CVD and then transferred onto target electrodes.

Preparation of MoS_2. The MoS_2 channels that we used were prepared by CVD growth and mechanical exfoliation. For the CVD method, we deposited MoS_2 on SiO_2/Si substrates using sulfur and MoO_3 powder as the precursors. The typical growth temperature was 850 °C, and argon was used as the carrier gas. For mechanical exfoliation, we exfoliated a MoS_2 sample with several layers from a MoS_2 mineral.

Fabrication of Devices. Electrodes, test holes, and conductive channels were all defined using standard photolithography. Electrodes for the CNT-TFTs were 50 nm thick Pd layers, and the conductive channels were patterned using O_2 plasma etching. Electrodes for the MoS_2 FETs were 50 nm thick Au layers. It also needs to be said that the same results are achieved when using Pd electrodes for MoS_2 FETs while using Au electrodes for CNT TFTs. The asymmetric channels of MoS_2 were fabricated using a site-specific method to transfer few-layer MoS_2. All buried electrodes here were fabricated by filling the SiO_2 holes which is etched by CF_4 reacting ion etching under the condition of 40 sccm, 2 Pa, and 50 W, and the speed is about 1 nm/(1.6 s).

Characterization of Electrical Properties. All electrical measurements were performed using a semiconductor analyzer (4156C, Agilent, USA) with a probe station (TTP, Lakeshore, USA) under specific conditions. The output waves of the rectifying circuits were captured using a digital oscilloscope (TDS2012C, Tektronix, USA).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b04076.

MoS_2 field-effect transistor, carbon nanotube thin film transistor, ambipolar aligned-array CNT-TFT and single-CNT transistor, comparison of I_{on} and resistance with channel length, electrical performance of MoS_2 Schottky barrier diode, characterization of exfoliated and CVD growth MoS_2, and comparison of transfer characteristics of MoS_2 FETs (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: qunqli@mail.tsinghua.edu.cn.

ORCID

Qunqing Li: 0000-0001-9565-0855

Notes

The authors declare no competing financial interest.

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